ABSTRACT

The image processing apparatus according to the present invention comprises: DMA control means 112 having image input/output processing means 100, an external memory 111, DMA setting holding means 113, address generating means 114, DRAM control means 115, DMA request generating means 119, and DMA request adjusting means 120; a processor 116 including encoding/decoding processing means 117; and a DMA bus 118 as shown in figure 1.

In the image processing apparatus so constructed, a transfer data group which can be previously subjected to DMA scheduling is divided into burst transfer units, and the DMA request generating means periodically issues the DMA request in the burst transfer units and performs DMA of the transfer data which cannot be subjected to the DMA scheduling during the period that the DMA of the transfer data is not performed, thereby avoiding concentration of specific DMA.